## REMARKS

Claims 32, 37, 49 and 52 have been amended to overcome various rejections under U.S.C. §112. No new issue of patentability is raised. Entry of the amendments under 37 C.F.R. 1.116 is proper. Reconsideration of this application is respectfully requested.

**Objection to drawings**

The Action objects to the drawings under 37 CFR 1.83(a). The Examiner alleges that the drawings of this application do not support "one of said second regions of said second conductivity dopant type is disposed between said alternating array and a top one of said first regions, and another of said second regions is disposed between said alternating array and a bottom one of said first regions" as recited in Claim 32. Applicant respectfully disagrees. In FIG. 5D, one of said second regions (e.g., 20D) of said second conductivity dopant type is disposed between said array (e.g., 28D) and a top one of said first regions (e.g., 18D), and another of said second regions (e.g., 20D) of said second conductivity dopant type is disposed between said array (e.g., 28D) and a bottom one of said first regions (e.g., 18D). This feature is also described in the Specification at, for example, Page 9, Line 19 to Page 10, Line 6. Reconsideration and withdrawal of the drawing objection are respectfully requested.

**Claim rejections under 35 U.S.C. §112**

The Action rejects Claims 32-33, 35, 37-38 and 47-55 for containing subject matter not described in the specification. The Examiner alleges that the phrase "one of said second regions of said second conductivity dopant type is disposed between said alternating array and a top one of said first regions, and another of said second regions is disposed between said alternating array and a bottom one of said first regions" is not supported in the original specification. The Applicant respectfully disagrees. As discussed above, the features included in these claims are supported by FIG. 5D and the Specification (Page 9, Line 19 – Page 10, Line 6) in sufficient detail for one of ordinary skill in the art to possess the claimed invention.

The Action rejects Claims 32-33, 35, 37-38 and 47-55 as being indefinite for reciting "alternating array." Claims 32 and 49 have been amended to recite that "the third regions are alternatingly arranged in an array within the third semiconductor layer" as shown in, for

example, FIGS. 2 and 5D. The claims also recite that the plurality of third regions are "laterally spaced." It is submitted that this recitation of laterally spaced third regions alternatingly arranged in an array within the third semiconductor layer is sufficiently definite to one of ordinary skill in the art.

The Action rejects Claims 32-33, 35, 37-38 and 47-55 as being indefinite for reciting N "corresponds" to the number of multiple bipolar transistors. Claims 32 and 49 have been amended to recite that N "is" the number of multiple bipolar transistors.

The Action rejects Claims 36 and 52 for indefiniteness. The Applicant believes that the Examiner meant to reject Claim 37, rather than Claim 36, as Claim 36 was previously cancelled and Claim 37 includes the feature referenced by the Examiner. Claims 37 and 52 have been amended to recite "box shaped," as recited in the description of the drawing of FIG. 5D and found in the Specification, Page 9, Line 21.

It is submitted that the foregoing amendments address each § 112 rejection set forth in the Action. Reconsideration and withdrawal of the § 112 rejections are respectfully requested.

**Claim rejections under 35 U.S.C. §102(b)**

The Action rejects Claims 32-33, 37-38, 47-50 and 52-55 as being anticipated by U.S. Patent No. 5,850,095 to Chen et al. under 35 U.S.C. §102(b). Claims 32 and 49 include features similar to those claimed in issued Claim 12 of the parent patent, U.S. Patent No. 5,850,095. To that end, the Applicant repeats herein the arguments which the Examiner found persuasive in allowing Claim 12 of the parent patent. Reconsideration and withdrawal of the rejection of Claims 32 and 49 in view of the following arguments are respectfully requested.

Referring to Chen et al., Fig. 5, the protection circuit relies on an SCR device 80 in conjunction with an additional base resistor R 36 in series with the inherent bipolar base resistors for device activation. Indeed, this is shown in detail in Chen et al. Fig. 3. As described in the referenced patent, column 2, line 38, "...the invention provides a[n] ... ESD circuit that is achieved through uniform turn-on of multi emitter fingers from an internal Zener diode current

source." Chen also provides that the Zener trigger circuit 30 includes a zener diode 32 that is coupled serially between pad 34 and resistor 36, column 3, lines 1-3.

Applicant's claimed invention does not require the additional devices to assure uniform turn on of multiple emitter fingers. This fact reduces the design and processing requirements of the claimed invention device over the Chen et al. structure. The claimed invention has a simpler, unique concept with less overall components, such as a Zener diode and associated resistor required by Chen et al.

The claimed invention achieves uniform turn on by the use of a unique emitter shape as depicted in Applicant's specification Figs. 5A-5D, and described in detail in Applicant's specification in the paragraph beginning on line 3 of page 8. Specifically referring to the sixth sentence beginning on line 12 of page 8, "The continuous serpentine emitter conductor 28A provides the capability of a single emitter current which provides a high assurance that all the base elements will conduct minimizing the possibility of localized device damage caused by excessive current, and therefore excessive joule heating, in any one transistor element. This provides good ESD protection while at the same time minimizing the device area."

It should be noted that Chen et al. states in column 1, line 51, "Moreover, when NPN transistors are used for ESD protection in sub-micron BiCMOS and CMOS applications, the ESD threshold level typically scales with the length of the emitter finger, and not with the number of provided fingers." This is typically caused by minute variations in process parameters that impede the ability for all the fingers to carry an equal share of the ESD current. Referring to Applicant's specification, the prior art is shown in Fig. 3 and Fig. 4. The Fig. 3 equivalent circuit shows four bipolar transistors in parallel between first and second voltage sources. It also shows the associated emitter-base resistors Rb1 through Rb4. It is desirable to have these resistances as identical as possible, but process variations make this difficult.

This is highlighted in Applicant's specification by the sentence beginning on line 21 of page 2, "However, there are still four different emitter fingers 28 in Fig. 4 in which process variation can cause slight differences in electrical characteristics as well as in the characteristics

of the base elements. This design structure therefore cannot always assure turn-on of all the emitter base elements to maximize the device ESD current capability." This is the reason ESD protection does not scale with the number of fingers.

In one embodiment, Applicant's claimed invention overcomes this drawback, without the use of extra components such as zener diodes, by using uniquely shaped emitters continuously connected to allow the ESD protection to scale with the length of the emitter.

As an example, the "box" shaped emitter claimed in dependent Claims 37 and 52 are shown in Applicant's Fig. 5D. This novel approach to improving ESD protection without using additional components is not anticipated by Chen et al. Although Claims 32 and 49 do not specifically describe the specific unique emitter shape of Applicant's claimed invention, it is required for device operation to have the elements described in those claims. The device structure must be taken in total to produce a functioning protection device with improved ESD capability. The collector and base elements together with associated contact regions are an integral part of a functioning device with unique emitter characteristics of the claimed invention.

In summary, Applicant's claimed invention has the uniqueness of the emitter construction that enables an electrical connection "on-chip". The base configuration and emitter configuration provide assurance that all elements of the device carry current during an ESD event. This provides the ESD protection efficiency of an extended length emitter without additional devices such as a zener element while maintaining a relatively compact device area.

It is also submitted that Applicant's claimed invention is not obvious from the disclosure of Chen et al. Indeed, Chen et al. teaches away from Applicant's invention by requiring additional components such as a zener diode and resistor. Further, Chen et al. does not describe in any way the shape of the emitter used.

In addition, Claims 32 and 49 have been amended previously to recite that "wherein said third regions are alternatingly arranged in an array within said third semiconductor layer, with 'N' number of said third regions, whereby 'N' is the number of multiple bipolar transistors in an

electrically parallel transistor array that comprise said ESD protection structure, and wherein one of said second regions of said second conductivity dopant type is disposed between said array and a top one of said first regions and, and another of said second regions is disposed between said array and a bottom one of said first regions."

The amended Claim 32 includes the features of previously cancelled Claim 36, which was only rejected in the previous action under 35 U.S.C. §112 (and which has been cured as argued above) and not based on any prior art, including Chen et al. It is submitted, therefore, that the Examiner has conceded the allowable subject matter in the Claim 32 as amended. Thus, reconsideration and withdrawal of the 102(b) rejection over Chen et al. are respectfully requested.

Notwithstanding the foregoing, Chen et al. does not disclose or suggest an ESD protection structure as claimed where said third regions are alternatingly arranged in an array within said third semiconductor layer, with "N" number of said third regions whereby "N" is the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

The Examiner now alleges that such feature in Claim 32 is met (a) by Chen's description and (b) by the inherent property of any NPN structure. The Applicant respectfully disagrees. Though Chen's background of the invention describes that NPN transistors are used for ESD protection, Chen et al. uses one third region to form the Zener diode 80, which is coupled to the first regions 58 as shown in Fig. 4. The Zener diode 80 is provided to lower the protection circuit trigger threshold, but not to function as a bipolar transistor in an ESD array for ESD protection. With such application, the Zener diode 80 is not a bipolar transistor in the electrically parallel transistor array that comprises the ESD protection structure. The number "N" of Chen's third region is not the number of multiple bipolar transistors. Thus, Chen's description fails to disclose or teach this feature of Claim 32.

Furthermore, Chen et al. purposefully uses the third region as the Zener diode 80 to lower the protection circuit trigger threshold, but not to function for ESD protection. Chen et al. thus teaches one skilled in the art to use a number of the third regions to form a different number of

bipolar transistors in the ESD protection structure. Chen's disclosure teaches away from the features of Claim 32 in which the number of the third regions is the number of multiple bipolar transistors. One of ordinary skill in the art, therefore, would not be motivated by Chen's descriptions to achieve this feature of Claim 32.

Further, Claim 32 was also previously amended to recite that wherein "one" of said second regions of said second conductivity dopant type is disposed between said array and a top one of said first regions and, and "another" of said second regions is disposed between said array and a bottom one of said first regions. Such recitation indicates that the second regions 20D are not disposed within the array as shown in FIG. 5D. On the contrary, Chen et al. forms second regions 64, which are referenced by the Examiner, between the second regions 56 as shown in Chen's Fig. 4. It is submitted that without disposing Chen's second regions as such, the desired ESD protection of Chen's structure cannot be achieved. Thus, Chen et al. fails to disclose or suggest forming the ESD structure with this additional feature recited in Claim 32. Therefore, it is submitted that Claim 32 is not anticipated by or obvious from Chen et al. and is allowable thereover.

Claims 33, 37-38 and 47-48 depend from Claim 32, and are, therefore, also not anticipated by Chen et al. for at least the same reasons discussed above.

Claim 49 recites the "N number of the third regions . . ." feature recited in Claim 32, which is discussed above. Claim 49, therefore, is also not anticipated by Chen et al. for at least the same reasons set forth in connection with Claim 32.

Claims 50 and 52-55 depend from Claim 49, and are, therefore, also not anticipated by Chen et al. for at least the same reasons set forth above.

**Objections for double patenting**

The Action rejects Claims 49-51 under 37 C.F.R. §1.75 as being a substantial duplicate of Claims 32, 33 and 35, respectively.

An applicant is entitled to restate his or her invention in a reasonable number of ways, and a mere difference in scope between claims has been held enough. *See* MPEP § 706.03(k). In preamble, Claim 32 recites ". . . ESD protection structure on a semiconductor substrate, functionally connected between an integrated circuit input or output pin and ground . . ." The scope of Claim 32 places the ESD protection structure between an integrated circuit input or output pin and ground. However, Claim 49 does not recite such limitation in the preamble. The ESD protection structure of Claim 49 can be, for example, functionally connected between other pins of an integrated circuit. Claim 49, therefore, has a different scope than that of Claim 32. Thus, it is submitted that Claim 49 is not a duplicate claim of Claim 32 and is allowable thereover.

Claims 50 and 51 depend from Claim 49, and should not be objected to for double patenting for at least the same reasons set forth above.

Accordingly, reconsideration and withdrawal of the double patenting objections are respectfully requested.

**Conclusion**

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Early notification to that effect is respectfully requested.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679.**

Respectfully submitted,

Dated: 3/20/06

Joseph A. Powers, Reg. No.: 47,006
Attorney For Applicant

DUANE MORRIS LLP
30 South 17th Street
Philadelphia, Pennsylvania 19103-4196
(215) 979-1842 (Telephone)
(215) 979-1020 (Fax)